EPFL

EMBEDDED SYSTEMS LABORATORY

A Ring Oscillator-based Analog-to-Digital Converter for X-HEEP

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Overview

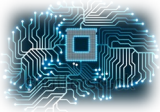
1. **Time-encoding technique: VCO-based ADC basis**
2. Targeting physio-bandwidth
3. Designing RO-based ADC for X-HEEP. **PROPOSAL**
4. Current Simulations

Technology evolution

Today's digital world

Biosensing/Sensors

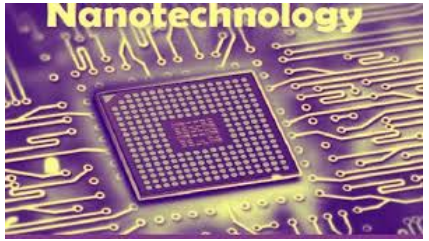
Neuromorphics circuits



Communications

Portable, small, cheap and high energy-efficient devices

Technology scaling * →



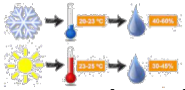
↓ Supply voltage

Lower voltage overhead

Digital circuits
- Higher operation speed
- Smaller area
- Lower power

Analog circuits
- Low intrinsic gain
- Higher noise impact
- Parasitic effects

temperature



humidity

pressure

Analog-to-Digital Converters

NEW DATA CONVERSION PARADIGMS

mostly digital implementations

Time-encoding A/D conversion →

Conventional A/D conversion technique: Amplitude-encoded

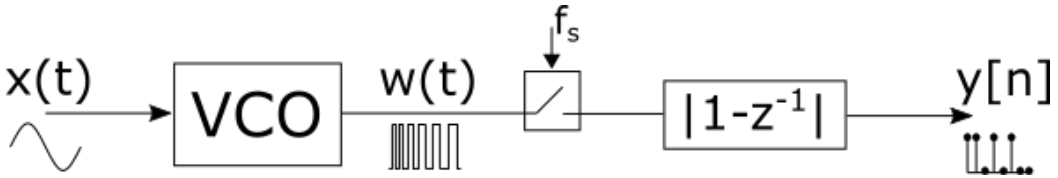
time events:
- time
- frequency
- phase

*L. L. Lewyn, T. Ytterdal, C. Wulff and K. Martin, "Analog Circuit Design in Nanoscale CMOS Technologies," in Proceedings of the IEEE, vol. 97, no. 10, pp. 1687-1714, Oct. 2009.

RO-based ADC basis

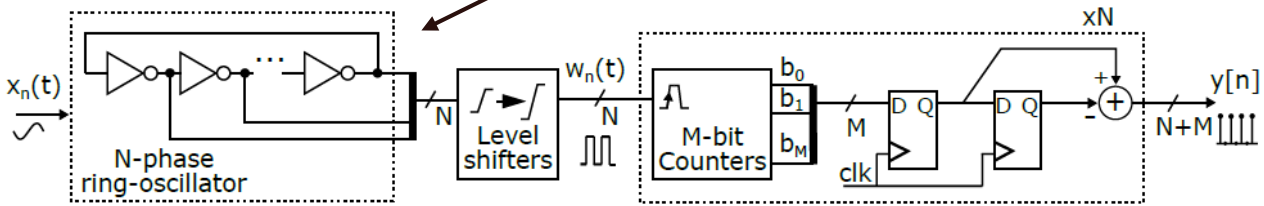
Time-encoding A/D conversion

Voltage-Controlled Oscillators-based ADCs



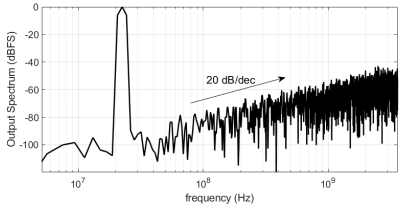
As a phase integrator

Ring Oscillators: a digital VCO



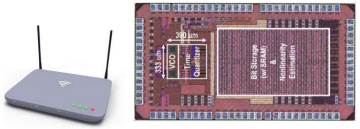
Open-loop configurations: simplest structure

1st order noise-shaped output data



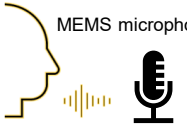
Applications

Communications

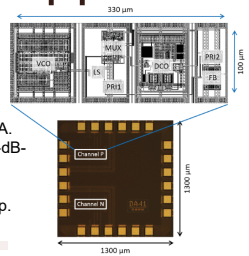


T. -F. Wu and M. S. -W. Chen, "A Noise-Shaped VCO-Based Nonuniform Sampling ADC With Phase-Domain Level Crossing," in IEEE Journal of Solid-State Circuits, vol. 54, no. 3, pp. 623-635, March 2019.

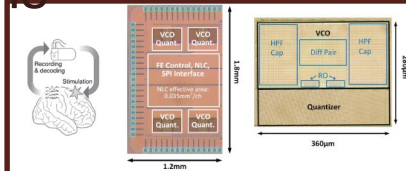
Audio



F. Cardes, E. Gutierrez, A. Quintero, C. Buffa, A. Wiesbauer and L. Hernandez, "0.04-mm2 103-dB-A Dynamic Range Second-Order VCO-Based Audio ΣΔ ADC in 0.13- μm CMOS," in IEEE Journal of Solid-State Circuits, vol. 53, no. 6, pp. 1731-1742, June 2018.

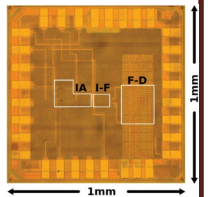


THIS WORK



W. Jiang, V. Hokhikyan, H. Chandrakumar, V. Karkare and D. Marković, "A ±50-mV Linear-Input-Range VCO-Based Neural-Recording Front-End With Digital Nonlinearity Correction," in IEEE Journal of Solid-State Circuits, vol. 52, no. 1, pp. 173-184, Jan. 2017.

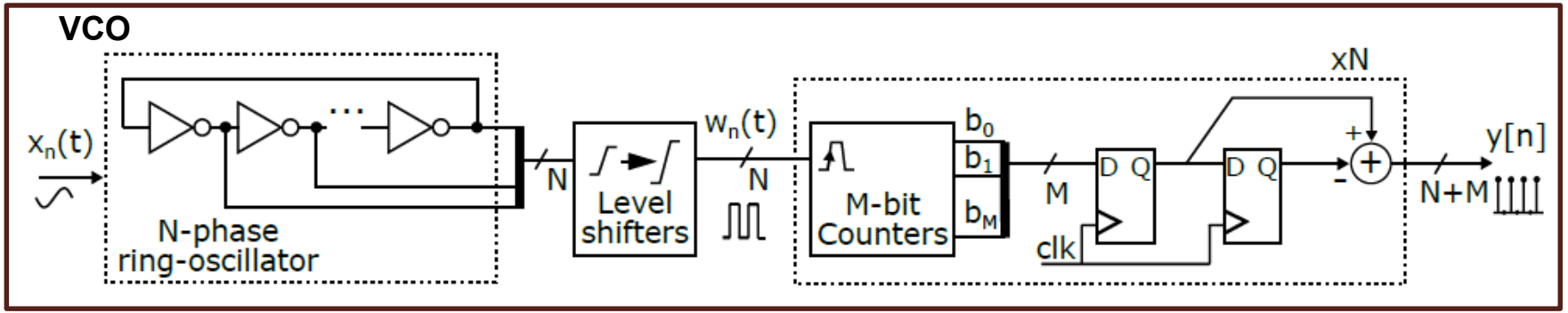
Sensing interface



O. Olabode et al., "Time-Based Sensor Interface for Dopamine Detection," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 10, pp. 3284-3296, Oct. 2020.

RO-based ADC basis

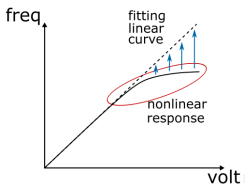
Open-loop VCO-based ADC



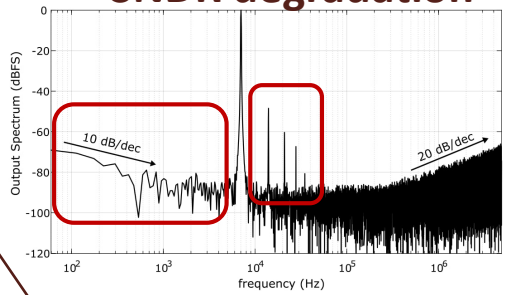
- Power and area savings
- Scalable designs
- P&R tools
- High sensitivity

*

- Nonlinear transfer function
- Phase noise



SNDR degradation

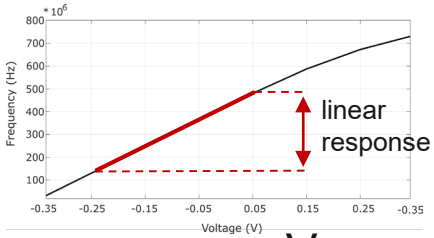


Way to linearize the RO response

RO design to reduce the phase noise

* W. Sansen, "1.3 Analog CMOS from 5 micrometer to 5 nanometer," 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, 2015, pp. 1-6.

Proposal: Several RO-based ADC paths

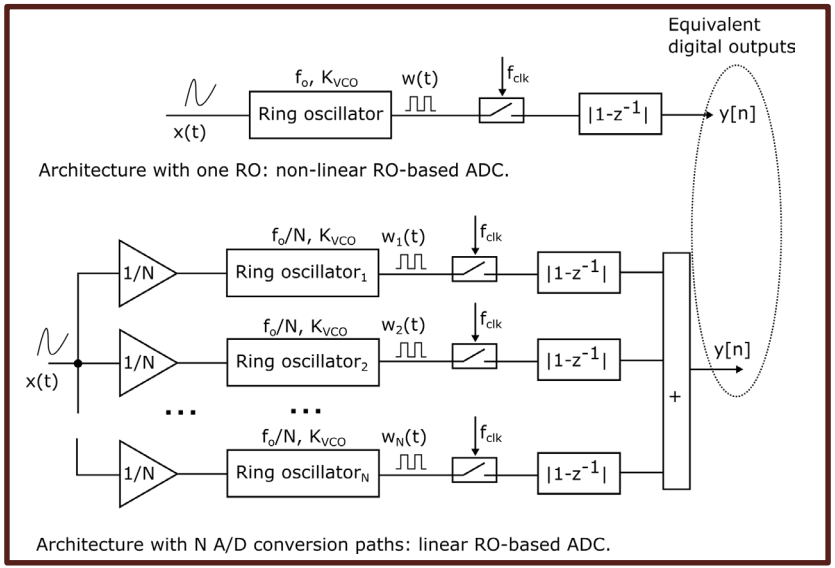


input signal attenuation:

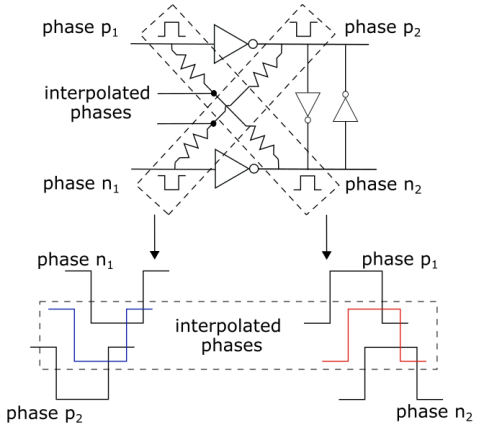
↓↓ K_{vco};

↑↑ Quantization noise.

*1



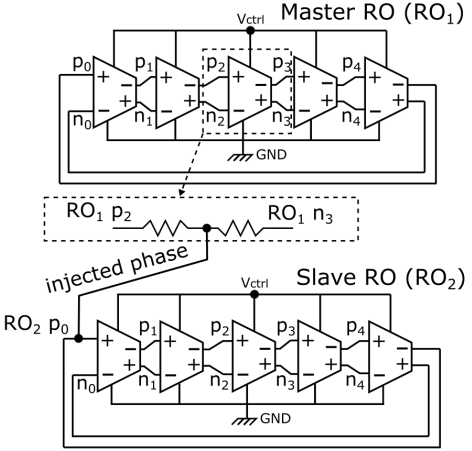
passive interpolation



Theoretically: *2

$$SNR_{improvement} = 6.02 \cdot log_2 \frac{N_{taps}{}'}{N_{taps}}$$

phase injection



Doubling taps

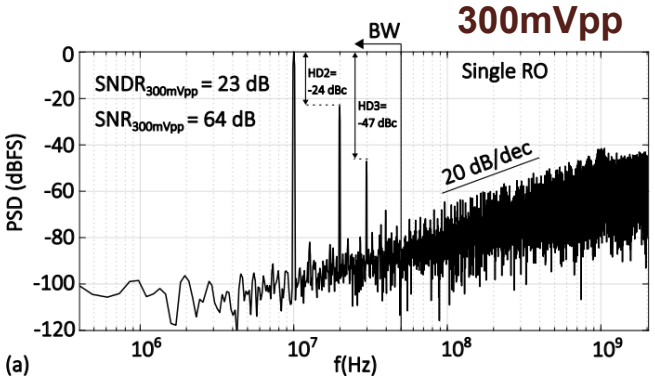
↓

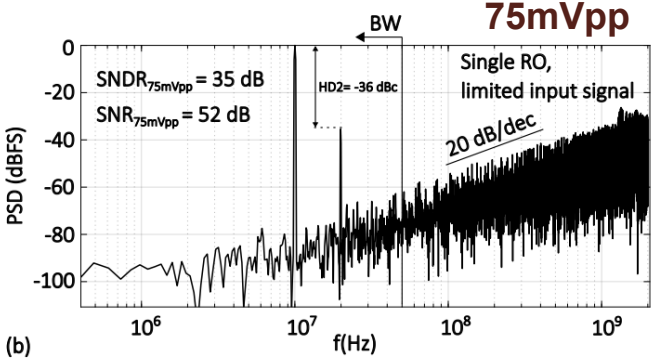
SNR enhances by 6dB

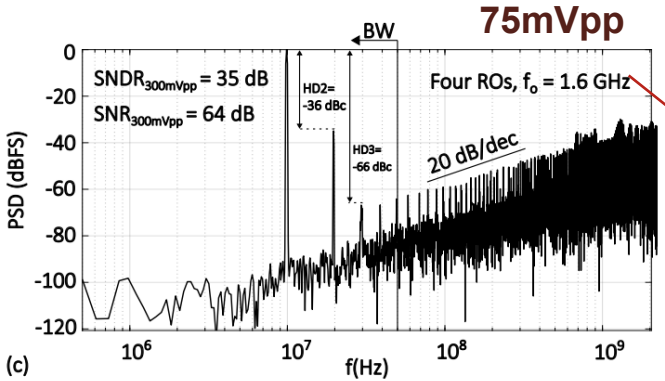
*1 Eric Gutierrez, Leidy Mabel Alvero-Gonzalez and Ruben Garvi, N Parallel Paths for Non-Linearity Mitigation in Ring Oscillator based Analog-to-Digital Conversion, accepted for publication on AEU – International Journal of Electronics and Communications.

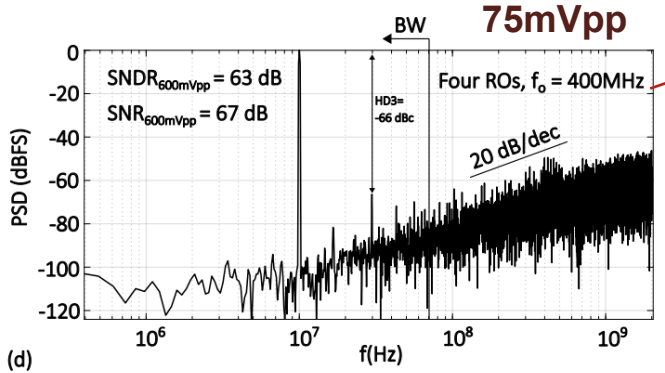
*2 E. Gutierrez, L. Hernandez, F. Cardes and P. Rombouts, "A Pulse Frequency Modulation Interpretation of VCOs Enabling VCO-ADC Architectures With Extended Noise Shaping," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 2, pp. 444-457, Feb. 2018.

Proposal: Several RO-based ADC paths



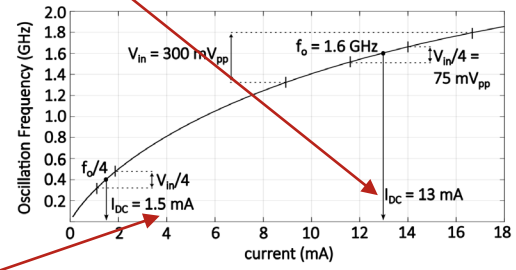






*

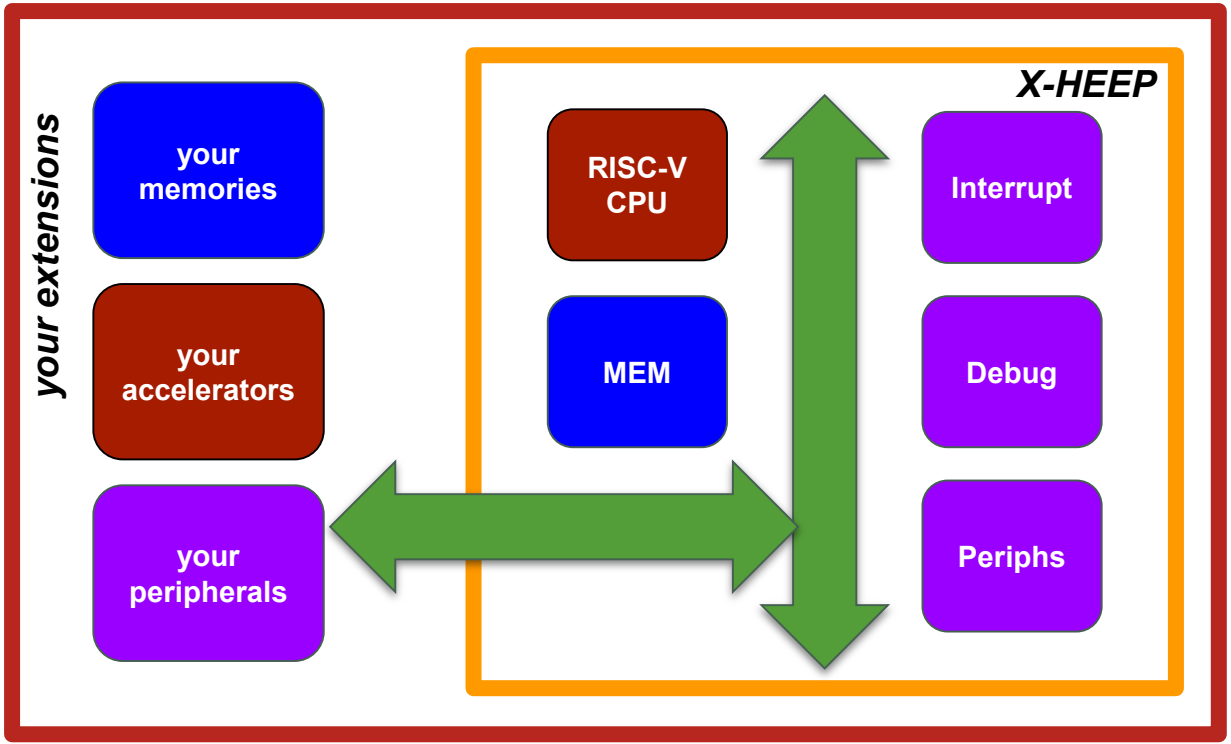
RO performance:



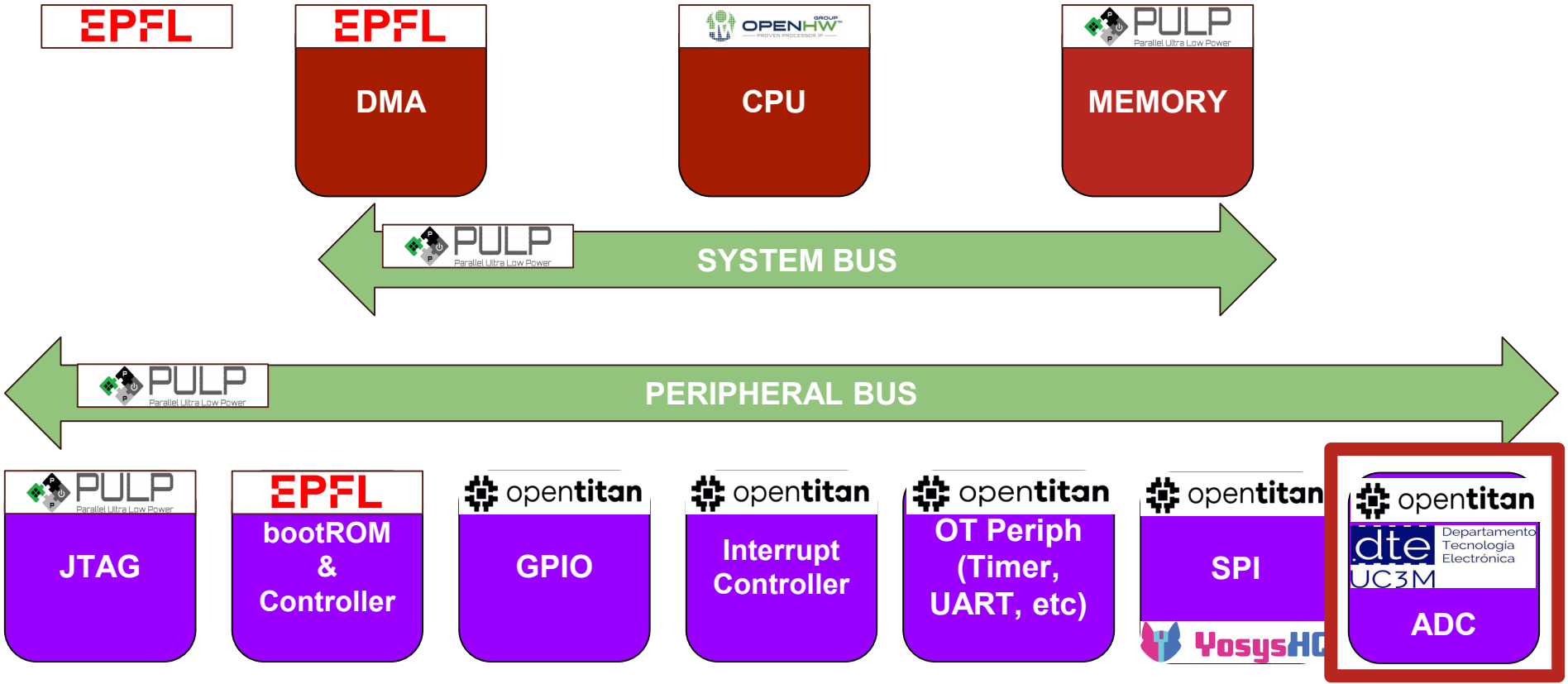
- No resolution degradation.
- Higher power-efficiency.
- More occupied area.

eXtendable Heterogeneous Energy Efficient Platform

Performance, Power and Energy Proportional Platform for Ultra-Low-Power Edge-Computing Applications



Practical application: X-HEEP



Specifications

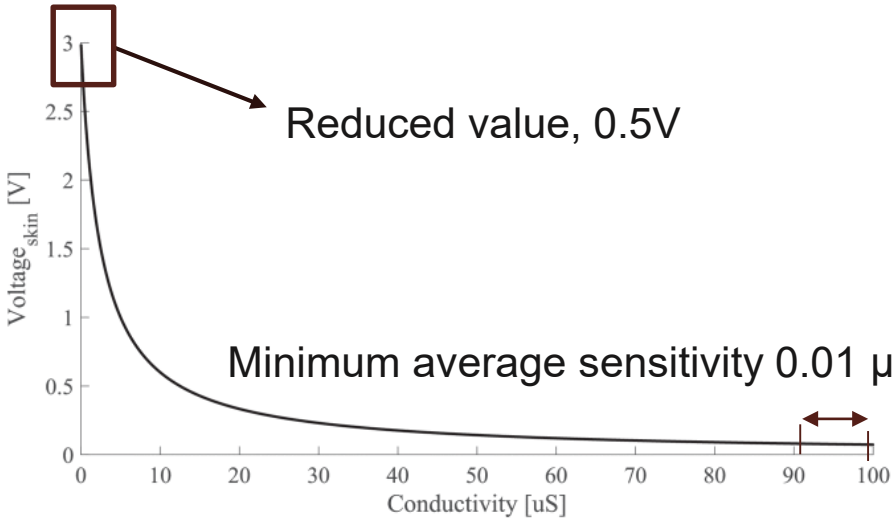
Biosignal: Electrothermal activity (EDA) or Galvanic Skin Response (GSR)

- Bandwidth (BW) = 1.5Hz
- DR: 14 ENOBs – 84dB
- Input signal: voltage
- Average sensitivity 0.01μS

Front-end circuit analysis

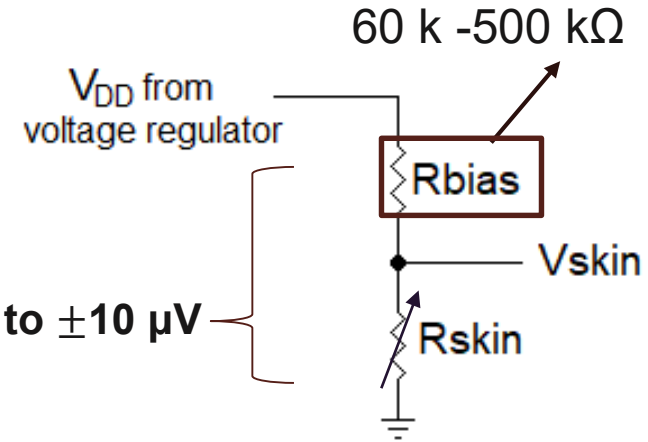
Maximum average current **9 µA**

*



Reduced value, 0.5V

Minimum average sensitivity 0.01 µS → **±1 µV to ±10 µV**



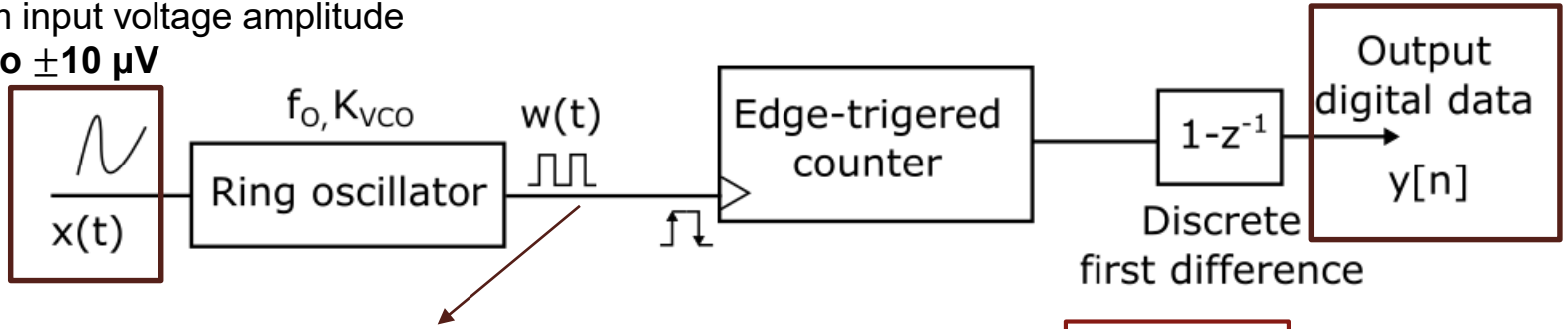
The sensitivity defines LSB of the ADC architecture.

* J. A. Miranda Calero, A. Páez-Montoro, C. López-Ongil and S. Paton, "Self-Adjustable Galvanic Skin Response Sensor for Physiological Monitoring," in *IEEE Sensors Journal*, vol. 23, no. 3, pp. 3005-3019, 1 Feb.1, 2023.

Designing an open-loop RO-based ADC

Minimum input voltage amplitude
± 1 μV to ±10 μV

1LSB → **Δy = 1**



Edges to be counted depends on the oscillation frequency range and the sampling frequency

$\Delta f_{osc}*N_{taps}/f_s \geq 1$ for the minimum input signal

$$\Delta f_{osc} = N_{taps} * K_{VCO} * \Delta V_{in} \geq f_s$$

$N_{taps}*K_{VCO} \geq f_s/\Delta V_{in}$

f_s = 250Hz → 250 MHz/V
f_s = 10Hz → 10 MHz/V
Feasible gain value

$$*SNR = 6.02 \cdot log_2\left(\frac{\Delta f_{osc} \cdot N_{taps}}{f_s}\right) - 3.41 + 30 \log OSR$$

↑↑ $f_{effective}$

$f_s/_{2BW}$

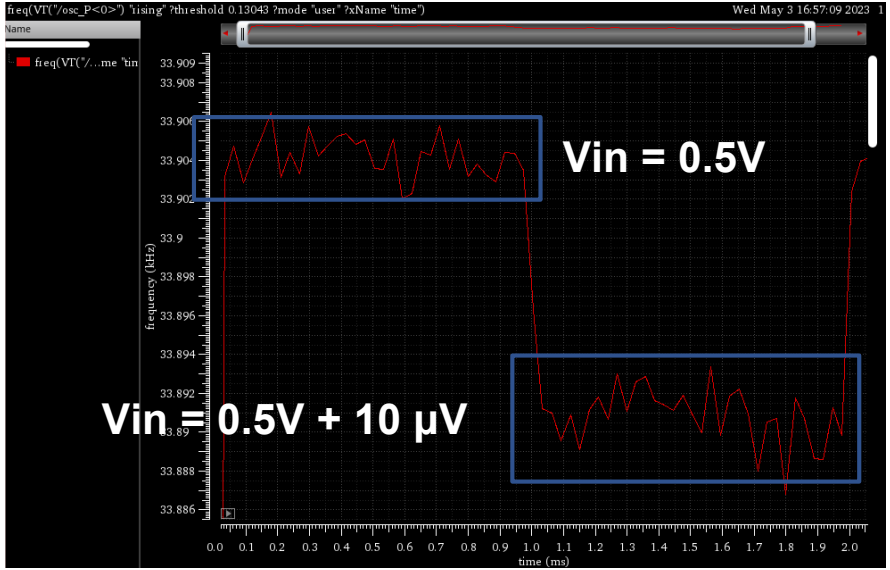
↑↑ f_s is not a limitation for low BW applications

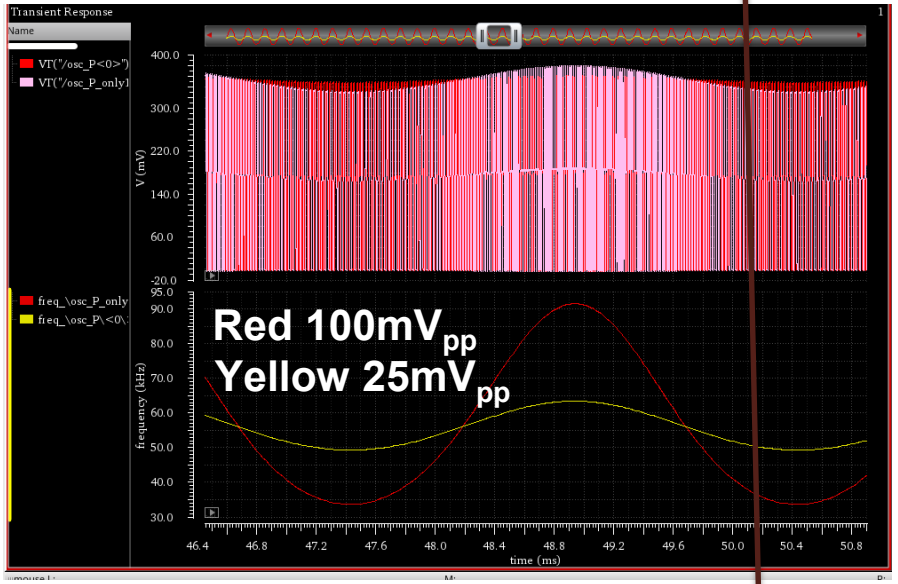
* Y. -G. Yoon, J. Kim, T. -K. Jang and S. Cho, "A Time-Based Bandpass ADC Using Time-Interleaved Voltage-Controlled Oscillators," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 55, no. 11, pp. 3571-3581, Dec. 2008.

Designing a RO: transistor level

Checked by Simulink/MATLAB model

Quantization noise = 100dB

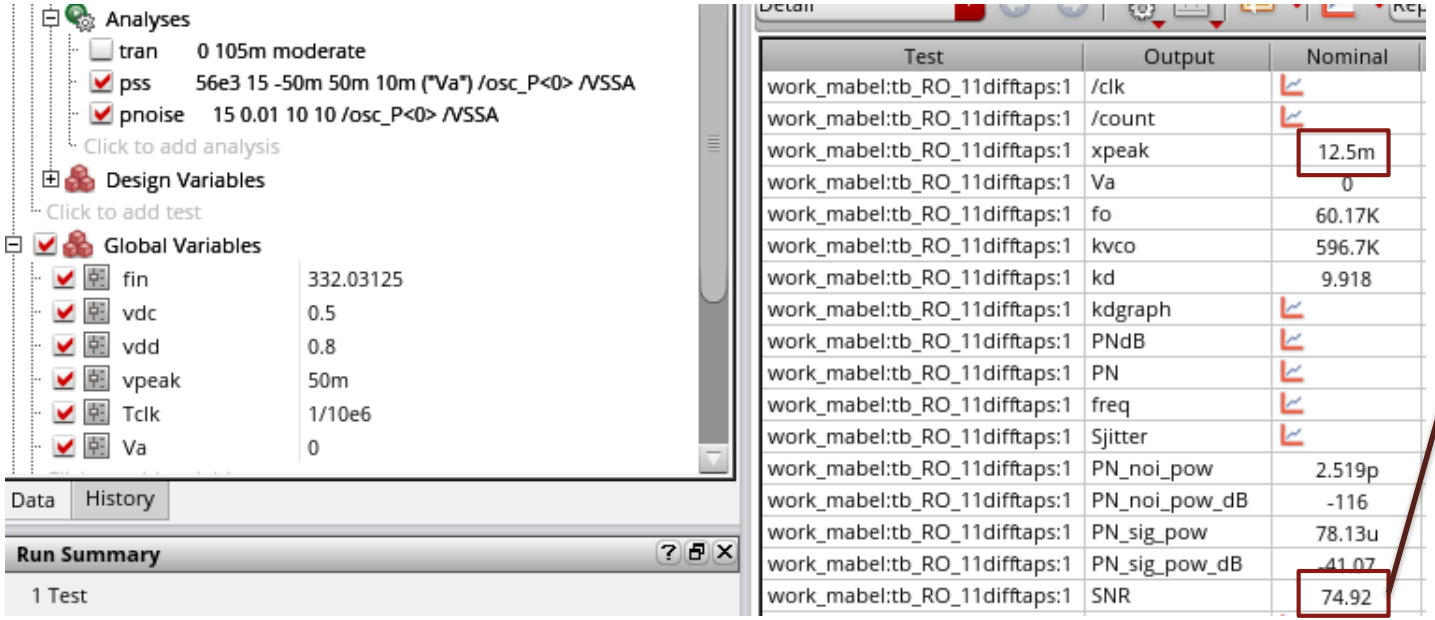




RO gain for 10 μV_{pp}
12 MHz/V for 20 phases from a single RO

The rest oscillation frequency, **f_o = 56kHz**;
RO gain in the entire input range, **K_{vco} = 560KHz/V**

Designing a RO: transistor level



Test	Output	Nominal
work_mabel:tb_RO_11difftaps:1	/clk	
work_mabel:tb_RO_11difftaps:1	/count	
work_mabel:tb_RO_11difftaps:1	xpeak	12.5m
work_mabel:tb_RO_11difftaps:1	Va	0
work_mabel:tb_RO_11difftaps:1	fo	60.17K
work_mabel:tb_RO_11difftaps:1	kvco	596.7K
work_mabel:tb_RO_11difftaps:1	kd	9.918
work_mabel:tb_RO_11difftaps:1	kdgraph	
work_mabel:tb_RO_11difftaps:1	PNdB	
work_mabel:tb_RO_11difftaps:1	PN	
work_mabel:tb_RO_11difftaps:1	freq	
work_mabel:tb_RO_11difftaps:1	Sjitter	
work_mabel:tb_RO_11difftaps:1	PN_noi_pow	2.519p
work_mabel:tb_RO_11difftaps:1	PN_noi_pow_dB	-116
work_mabel:tb_RO_11difftaps:1	PN_sig_pow	78.13u
work_mabel:tb_RO_11difftaps:1	PN_sig_pow_dB	-41.07
work_mabel:tb_RO_11difftaps:1	SNR	74.92

Phase noise = 74 dB

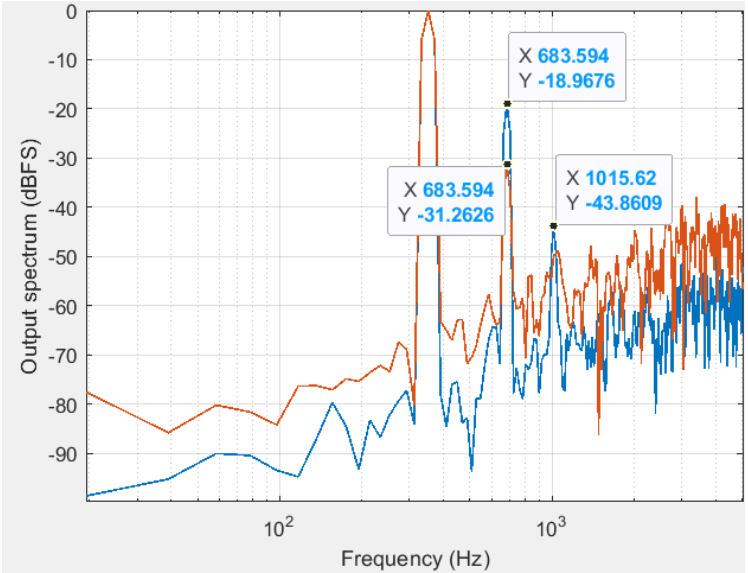
Thermal noise
- RO current

Flicker noise
- size of transistor
- Number of taps
- Matching edges

Phase noise domains over quantization noise

Designing a RO: transistor level

Nonlinearity performance

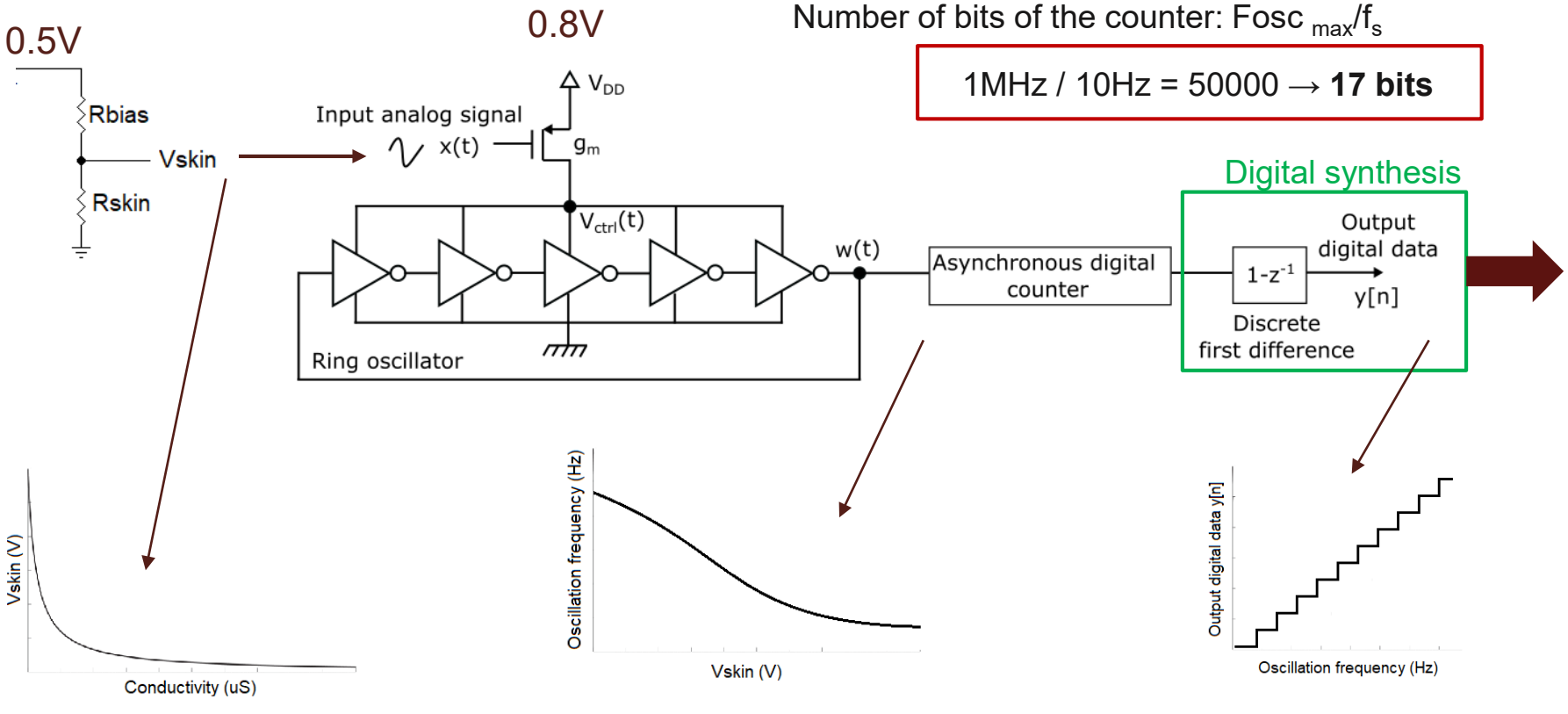


Transient simulations for f_{in} = 333 Hz and f_s = 10 kHz

Blue: Vin = 100 mV_{pp}
Orange: Vin = 25 mVpp

- More channels to reduce the distortion further
- Pseudo-differential ADC structure to remove the even harmonics terms.

Open-loop RO-based ADC for GSR



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by

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